

***Supporting Information For:***

# Encoding Active Device Elements at Nanowire Tips

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## **This file includes:**

Materials and Methods

Supplementary Figures S1-S7

Supplementary References

## Materials and Methods

**Synthesis of Si p-n junction tip-modulated nanowires.** The p-Si nanowire cores were grown epitaxially on Si (111) substrates (p-type, 3-5  $\Omega\cdot\text{cm}$ , Nova Electronic Materials) by Au-nanoparticle-catalyzed vapor-liquid-solid (VLS) process. 50 nm diameter Au nanoparticles (Ted Pella, Inc.) were suspended in 10% aqueous HF solution and were dispersed on Si (111) substrates, which were pre-etched with BHF (Buffered Oxide Etch 7:1, J.T. Baker) for 10 s. The VLS growth was carried out using silane ( $\text{SiH}_4$ ) (1-2 sccm), diborane ( $\text{B}_2\text{H}_6$ ) (14 sccm, 100 ppm in  $\text{H}_2$ ), and  $\text{H}_2$  (4-5 sccm) for 20-30 min at total pressure and temperature of 10 torr and 500  $^\circ\text{C}$ , respectively. Subsequently, the conformal  $\text{SiO}_2$  insulation layer ( $\sim 50$  nm) was deposited with atomic layer deposition (ALD, Savannah-S200, Cambridge NanoTech) at 250  $^\circ\text{C}$ . Next, the growth substrate was spin-coated with a protective resist layer (SU-8 2005 or 2010, MicroChem Corp.), which was prebaked at 95  $^\circ\text{C}$  for 3 min and then thinned using an oxygen plasma stripper (PJ-II, AST Products Inc., 50 W for 1-2 h) to expose the nanowire tips. The substrate was subsequently ultrasonicated (500D, Crest Ultrasonics) in isopropanol at 120 W for 1 min to remove the nanowire tips. After ultrasonication, the protective resist layer was removed by rinsing in acetone and an additional cleaning step using an oxygen plasma stripper (150 W for 1 h). Finally, the growth substrate was treated with BHF for 4 s and immediately transferred to the CVD chamber for the shell growth. The n-Si shell was deposited by flowing  $\text{SiH}_4$  (0.15 sccm),  $\text{PH}_3$  (0.15-0.75 sccm, 1000 ppm in  $\text{H}_2$ ), and  $\text{H}_2$  (60 sccm) for 3-14 min at total pressure and temperature of 25 torr and 775  $^\circ\text{C}$ , respectively.

**Material characterization.** Tip-modulated nanowires were imaged using Zeiss Ultra Plus field emission scanning electron microscope (SEM). For plan-view transmission electron microscope (TEM) imaging, as-synthesized tip-modulated nanowires were shear-transferred to p-type Si wafer. Cross-sections were prepared by deposition of a protective carbon layer and subsequently lifted out using a Zeiss NVision 40 dual-beam SEM/focused ion beam (FIB) equipped with an Omniprobe micromanipulator. The plane-view was characterized using an aberration-corrected Zeiss Libra MC TEM operating at 200 keV.

**Fabrication of tip-modulated nanowire devices.** As-synthesized Si p-n junction tip-modulated nanowires were shear-transferred to silicon nitride ( $\text{Si}_3\text{N}_4$ ) substrates (200 nm  $\text{Si}_3\text{N}_4$ /100 nm thermal  $\text{SiO}_2$  on n-Si, Nova Electronic Materials). The substrate was spin-coated with SU-8 (2000.5, MicroChem Corp.). Electron beam lithography (EBL) defined a pattern, which serves as an etch mask to protect the shell near the tip and the base of the nanowire. The substrate was dipped into BHF for 6 s and subsequently submerged into KOH (20 vol.% in water, 60 °C) for 40-60 s. The SU-8 etch mask was subsequently removed by UV-ozone stripper (UV-1; Samco International Inc., 300 °C for 40 min). MMA/PMMA resist layers (two layers of EL11 and one layer of C2, MicroChem Corp.) were spin-coated and EBL patterned the core and shell contacts. The substrate was treated with BHF for 50 s and then thermal evaporation (Ti/Pd, 3/450 nm) metallized the contacts.

**Electrical characterization.** I-V curves of the tip-modulated nanowire devices were measured with a probe station (TTP-4, Desert Cryogenics) and a digital-to-analog converter (DAC) card (PCI-6030E, National Instruments, Inc.) and with a semiconductor parameter analyzer (4156 C, Agilent Technologies). The tip-modulated nanowire devices were spin-coated with PMMA resist

layers (two layers of C5, MicroChem Corp.) EBL defined a window only near the nanowire tip.  $1\times$  phosphate buffered saline (PBS) solution was placed on top of the device substrate. Water-gate experiments were carried out with an Ag/AgCl reference electrode to apply the gate voltage ( $V_{wg}$ ). The source-drain current of the device was amplified by a current preamplifier (1211, DL Instruments) at sensitivity of  $10^{-6}$  or  $10^{-7}$  A/V, filtered (60 kHz, CyberAmp 380, Molecular Devices, Inc.), and digitized at 250 kHz sampling rate (Axon Digidata 1440A Data Acquisition System, Molecular Devices, Inc.). For spatial characterization of device sensitivity, nanowire devices were spin-coated with PMMA resist layers and EBL yielded a size-controlled window, which exposes a targeted length of nanowire tip. We recorded conductance response versus applied water-gate voltage and obtained a transconductance value. Subsequently, we removed the PMMA layer using acetone and oxygen plasma cleaning. We repeated this experiment by changing the size of the PMMA window and exposing different lengths of the nanowire tip. To assess the temporal response of the tip-modulated nanowire devices, a pulsed water-gate with rise time and duration of 0.1 ms and 1 ms and amplitude of 100 mV was generated (Axon Digidata 1440A Data Acquisition System, Molecular Devices, Inc.) and the current of the device was amplified with a home-built current preamplifier, filtered (60 kHz, CyberAmp 380, Molecular Devices, Inc.), and then digitized (Axon Digidata 1440A Data Acquisition System, Molecular Devices, Inc.).

**Optical characterization.** A Si p-n junction tip-modulated nanowire device was mounted on a piezo-controlled movable stage (Digital PI PZT flexure stage) to precisely control the nanowire tip position. The device was optically pumped at room temperature by a 488 nm Ar-ion continuous wave (CW) laser, which was focused onto a spot of  $\sim 1.6\ \mu\text{m}$  in diameter using a  $\times 40$  microscope objective lens with a numerical aperture (N.A.) of 0.65. Device bias voltage and

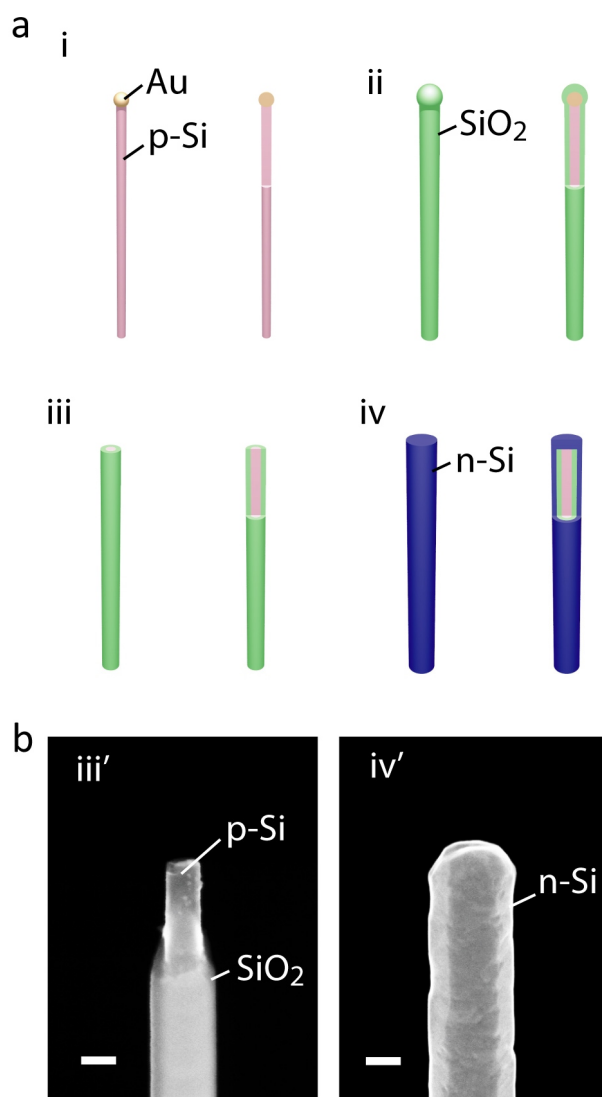
current were measured under laser illumination or in the dark using a semiconductor parameter analyzer (4156 C, Agilent Technologies) as the laser spot was aligned to the nanowire tip or scanned across the device. The total laser power was measured using a power meter (1918-C, Newport) and the incident illumination power was obtained by considering the area fraction of the nanowire within the laser spot when the tip is aligned to the center of the spot. The device responsivity was obtained by dividing the measured photocurrent by the incident illumination power. In scanning photocurrent measurement, the photocurrent was recorded while the incident laser spot was line-scanned across the nanowire. Incident illumination power was  $\sim 28.1 \mu\text{W}$ . The scanning step size was 300 nm for both x- and y-directions. For nanowire tip masking experiment, the device was spin-coated with MMA/PMMA layers (two layers of EL11 and one layer of C2, MicroChem Corp.). EBL defined mask pattern at the nanowire tip. A 100-nm-thick  $\text{Si}_3\text{N}_4$  layer and a 350-nm-thick Al metal layer were then deposited using plasma-enhanced chemical vapor deposition (PECVD, Nexx Systems) and thermal evaporation, respectively. The same illumination conditions used before tip masking were applied after tip masking.

**Top-down/bottom-up synthesis of vertical tip-modulated nanowire arrays.** Si (111) substrates (p-type, 0.001-0.005  $\Omega \text{ cm}$ , Nova Electronic Materials) were spin-coated with a SU-8 (2002, MicroChem Corp.) resist. EBL or photolithography was used to define hole arrays with circular cross-sections and diameters of  $\sim 1.5 \mu\text{m}$ . Then the substrate was hard-baked at 180  $^\circ\text{C}$  for 20 min. The substrate underwent deep reactive ion etching (SPTS Rapier DRIE, SPTS Technologies), and the oxygen plasma stripper at 150 W for 30 min cleaned residual resist on the substrate. The substrate was dipped into KOH (20 vol.% in water, 60  $^\circ\text{C}$ ) until the diameters of nanowires were reduced to 300-400 nm. The substrate was coated with  $\text{SiO}_2$  (50 -200 nm) by

ALD. The substrate was spin-coated with a SU-8 (two layers of 2010, MicroChem Corp.) resist with thickness ca. 20  $\mu\text{m}$ . Oxygen plasma stripper (50 W for 30 min-1 h) was used to partially etch and reduce the height of the SU-8 until the nanowire tips with length of ca. 4  $\mu\text{m}$  were exposed. The substrate was put in isopropanol and treated with ultrasonication at 120 W for 1 min. The remaining SU-8 was removed by oxygen plasma stripper (100 W for 1-2 h). The substrate was treated with BHF for 4 s and immediately transferred to the CVD chamber for the n-Si shell growth. The n-Si shell was deposited by flowing  $\text{SiH}_4$  (0.15 sccm),  $\text{PH}_3$  (0.15-0.75 sccm, 1000 ppm in  $\text{H}_2$ ), and  $\text{H}_2$  (60 sccm) for 14 min at total pressure and temperature of 25 torr and 775  $^\circ\text{C}$ , respectively.

**Fabrication of vertical tip-modulated nanowire device arrays.** The top-down/bottom-up synthesis described above was used to fabricate a  $10 \times 10$  array of nanowire devices, where each device consists of a  $2 \times 2$  array of vertical tip-modulated nanowires, on Si chip with a size of 2 cm  $\times$  5 cm. For the subsequent device fabrication, photolithography was used to selectively pattern a SU-8 mask (two layers of 2010, MicroChem Corp.) on top of each  $2 \times 2$  nanowire subset to protect the n-Si shell around the nanowires. Next, the unprotected parts of the n-Si shell on the substrate were etched by KOH (30 s, 20 vol.% in water, 60  $^\circ\text{C}$ ). The SU-8 resist was removed by rinsing in acetone and an additional oxygen plasma cleaning step (150 W for 1 h). The common core contact pad and the individual shell contact pads were then patterned by photolithography. The pattern for common core contact pad was located at  $\sim 2.8$  cm away from the center of the  $10 \times 10$  array of nanowire subsets. A section of substrate, where the common core contact is located, was partially dipped into BHF (50 s) to remove ALD deposited  $\text{SiO}_2$  layer. Finally, the whole substrate was briefly treated with BHF (4-8 s) and quickly transferred to

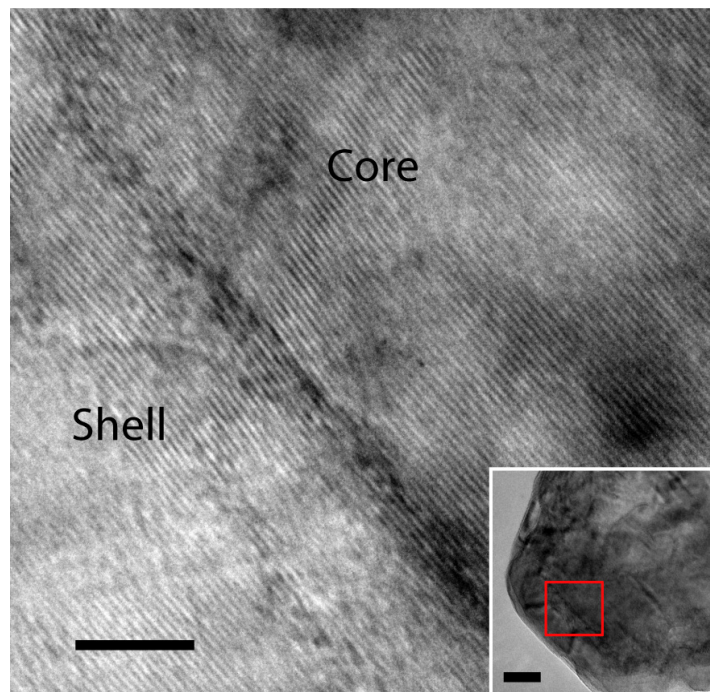
a thermal evaporator for metallization of the core and the shell contacts (Ti/Pd, 3/120 nm) to yield the vertical tip-modulated nanowire device arrays.



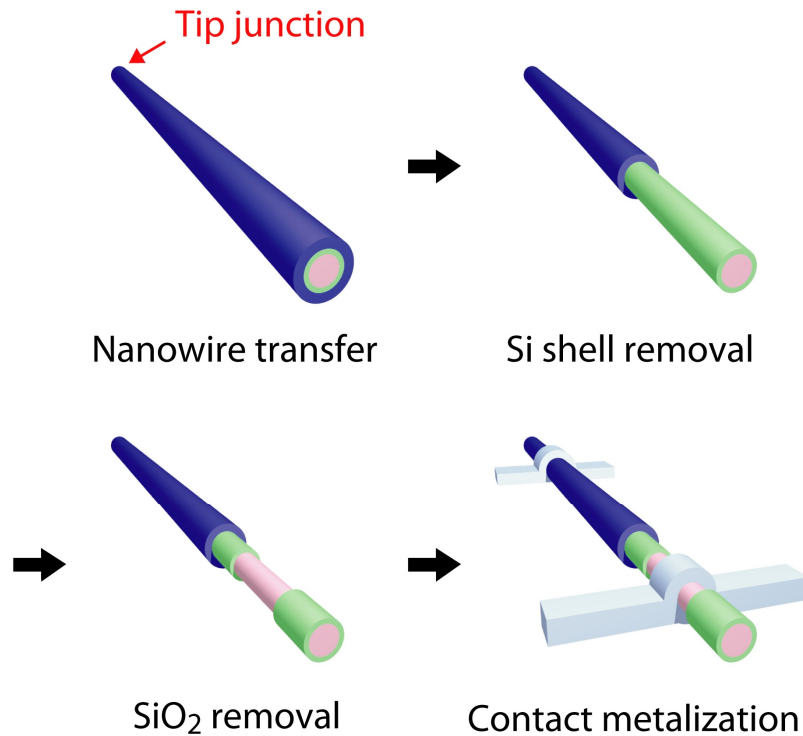
**Figure S1. Tip-modulated nanowire synthesis.** (a) Schematics highlighting key steps in the bottom-up synthesis of tip-modulated nanowires with a p-n junction at the Si nanowire tip. Steps (i)-(iv) correspond to the same steps described in Figure 1b of the main text. The right panel in each schematic illustrates the partially half-cut structure of the nanowires in order to more clearly visualize variations in composition across the diameter and tip of the nanowire at different stages for synthesis. (b) SEM images of steps (iii) and (iv). The SiO<sub>2</sub> layer was etched back 300 – 400 nm with BHF after mechanical tip removal (iii') and the n-Si shell was subsequently deposited to yield the tip-modulated nanowire (iv'). The BHF etch-back allows for additional control of the



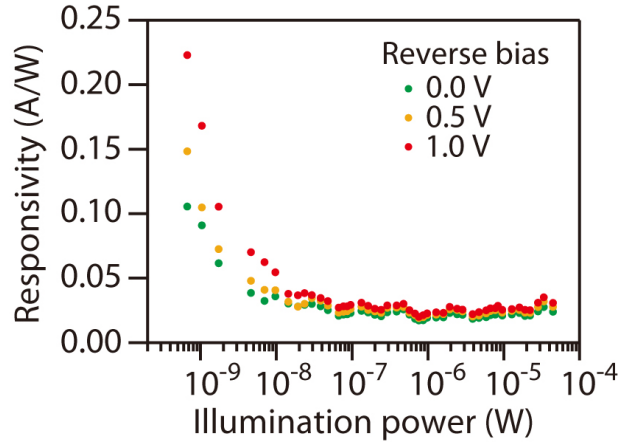
tip junction area and morphology of the nanowire through variations in the BHF etching time in (iii'). Scale bars, 100 nm.



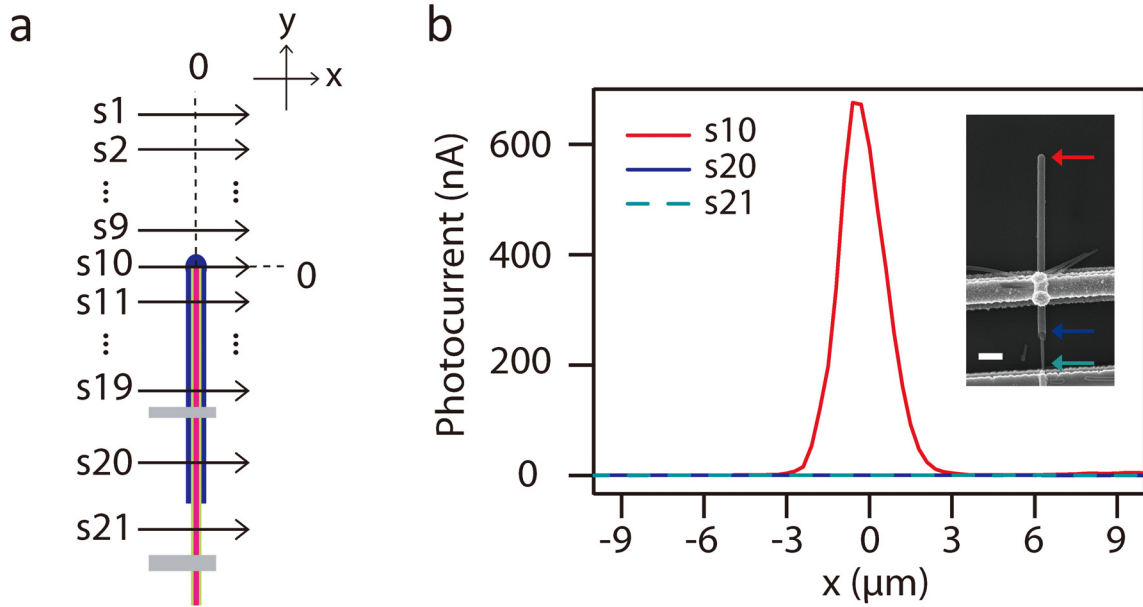
**Figure S2. High resolution transmission electron microscope (HRTEM) image of a nanowire tip-junction (n-type shell growth time, 3 min).** Scale bar, 5 nm. Inset shows the lower magnification bright-field TEM image of tip of the same nanowire. The red box specifies the area for the HRTEM image. Scale bar, 20 nm. The imaging of the tip-junction reveals a clean interface between the p-type core and n-type shell.



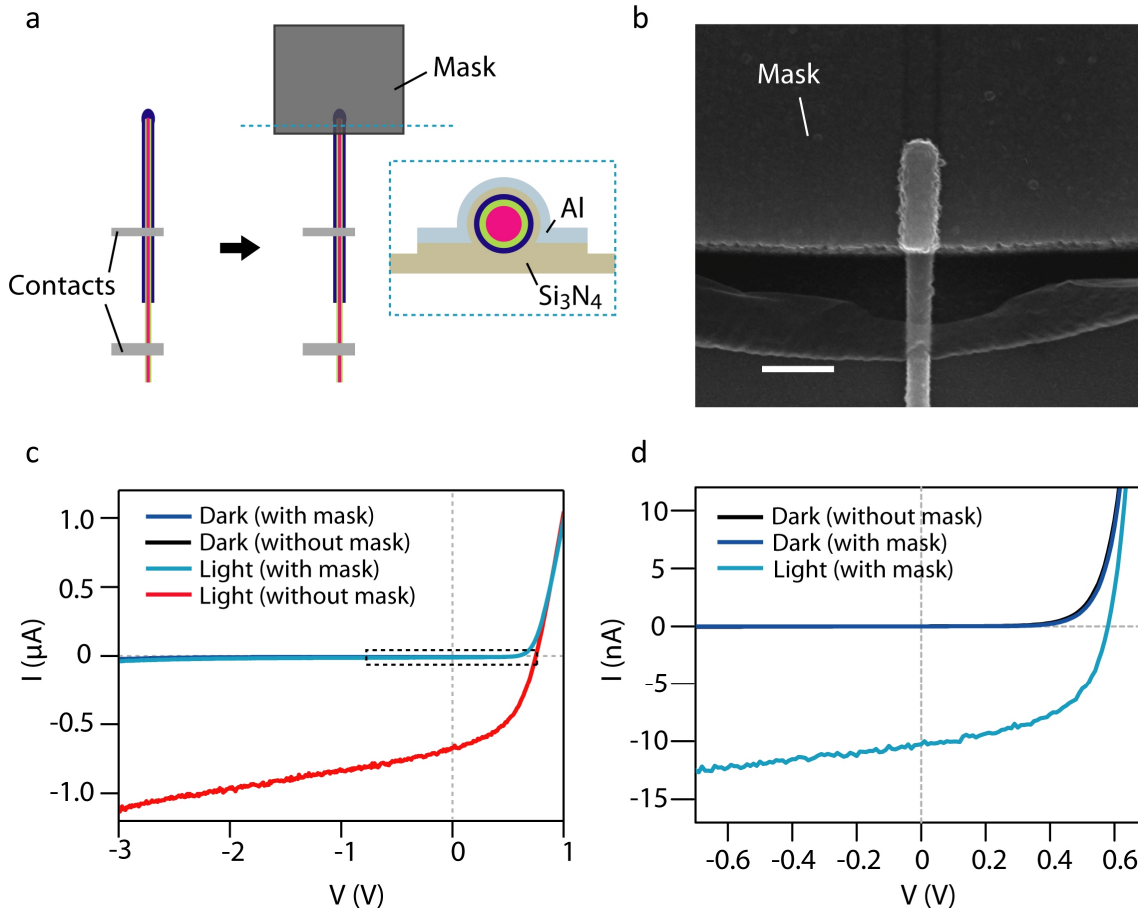
**Figure S3. Schematics showing key steps in the fabrication of a tip-modulated nanowire device.** Tip-modulated nanowires were transferred to a Si chip with SiO<sub>2</sub> (100 nm) and Si<sub>3</sub>N<sub>4</sub> (200 nm) passivation layers (top left, substrate not shown); the uppermost Si<sub>3</sub>N<sub>4</sub> was used to minimize etching during processing. The nanowire was protected with SU-8, and the end opposite the tip junction (junction position, red arrow) was exposed following electron-beam lithography. The n-Si shell (blue) in this open window was removed by KOH etching to expose the underlying SiO<sub>2</sub> shell (green, top right). Next, an additional electron-beam lithography step was carried out to open a second smaller window in this region, and then the unprotected SiO<sub>2</sub> layer in this window was removed by BHF etching to expose the p-Si core (pink, bottom left). Finally, an third step of electron-beam lithography and metallization (Ti/Pd, 3/450 nm) was carried out to define individual contacts (bright gray, bottom right) to the core and shell components to yield the tip-modulated nanowire device.



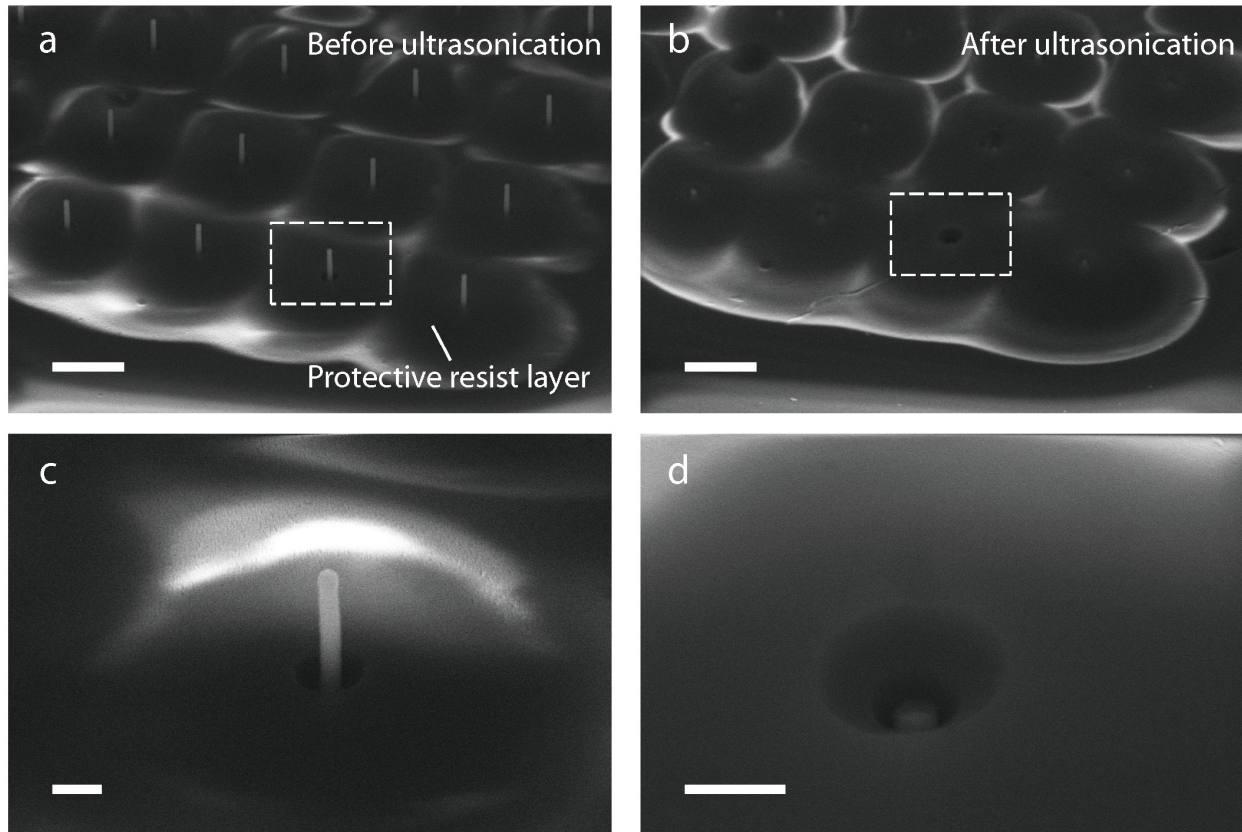
**Figure S4. Device responsivity.** Responsivity plotted as a function of illumination power (488 nm laser) for reverse bias voltages of 0 (green), 0.5 (orange) and 1.0 V (red). The responsivity was calculated as the ratio of the measured photocurrent (Figure 3c) to the incident illumination power for a given reverse bias voltage. The maximum responsivity of  $\sim 0.22$  A/W was measured at an incident power of 0.7 nW and a reverse bias voltage of 1.0 V. The increase in responsivity with increasing reverse bias voltage at fixed illumination power is consistent with previous results reported for nanowire photodetectors.<sup>S1</sup>



**Figure S5. Scanning photocurrent measurements.** (a) Schematic illustration of line-scans through the tip-modulated nanowire device, with p-Si core (red), SiO<sub>2</sub> insulating inner shell (light green), and n-Si outer shell (blue); the contact positions are indicated by horizontal gray bars below s19 and s21 scan lines. (b) Selected line-scan measurements through the nanowire tip (s10, red solid line) and core/shell (s20, blue solid line) and core only (s21, green dashed line) positions between the core and shell contacts. Measured photocurrent peaks were ~680 (tip, s10), ~0.28 (core/shell, s20), and ~0.12 nA (core only, s21), respectively. The same nanowire device as the one in Figure 3 was used. The incident illumination power was ~28.1 μW for all line-scans. Inset, SEM image of the nanowire device on a Si<sub>3</sub>N<sub>4</sub>-terminated silicon substrate. The red, blue, and green arrows indicate the nanowire tip (s10), core/shell (s20, 7.8 μm in y direction from the tip), and core only positions (s21, 9.2 μm in the y direction from the tip), respectively. Scale bar, 1 μm.



**Figure S6. Light and dark I-V curves before and after the tip-masking.** (a) Schematics showing masking of the nanowire tip by a 100 nm Si<sub>3</sub>N<sub>4</sub> and 350 nm Al mask described previously.<sup>S2</sup> The inset shows the cross-section of the nanowire along the dashed blue line after deposition of the mask. (b) SEM image of a masked nanowire tip. The length of nanowire tip region that is masked is ~1.5 μm. Scale bar, 1 μm. The same nanowire from Figure 3 was used. (c) Light and dark I-V curves of the same nanowire device before (red and black curves) and after (cyan and dark blue curves) the tip-masking. The same conditions for laser illumination, ~28 μW incident power, were used to record response of the masked and unmasked (Figure 3b) device. (d) Magnified view of the I-V curves around 0 V bias, specified by the dashed box in (c). A ca. 65-fold lower photocurrent is observed with 1.5 μm of tip masked. Small photocurrents can be attributed to scattering at the boundary of the mask, which couples a small portion of laser light through the Si<sub>3</sub>N<sub>4</sub> dielectric layer to the tip junction. Overall, the masking experiments confirm that photocurrent generation is localized primarily at the nanowire tip junction.



**Figure S7. Mechanical removal of nanowire tips.** (a-b) Low magnification SEM images (45 degree tilt) of the vertical nanowire arrays with a protective SU-8 layer, before (a) and after (b) the ultrasonication step in Figure 4a (IV). (a) Nanowires with exposed lengths of ca. 4  $\mu\text{m}$  are observed after 1-hour oxygen plasma stripping of the protective resist layer with a thickness  $>20$   $\mu\text{m}$ . (b) The exposed parts of nanowires were broken while the nanowire parts inside the resist were protected. The ultrasonication process with 120 W was performed for 1 min. Scale bars, 5  $\mu\text{m}$ . (c-d) Higher magnification SEM images of single nanowires (white dotted boxes in (a) and (b)) before (c) and after (d) the ultrasonication step. Scale bars, 1  $\mu\text{m}$ . The images show successful mechanical removal of the nanowire tips, which ensures exposure of p-Si cores at nanowire tips for the subsequent junction formation in the subsequent step of n-Si shell deposition.

## Supplementary References

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2. Tian, B. Z.; Zheng, X. L.; Kempa, T. J.; Fang, Y.; Yu, N. F.; Yu, G. H.; Huang, J. L.; Lieber, C. M. *Nature* **2007**, *449*, 885-889.